Design and Implementation of 32-Bit ETA Using OR Gate

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Abstract: *As the technology is progressing day by day, demand of gadgets are also very increasing according to the requirements. Adder is basic block of any digital circuitry, if these blocks give best results in terms of area, power and delay hence overall performance of the system will increase. As the size is reducing, Low power devices are in great demand. Here we design ETA in which accuracy will remain same as before but approximate part is modified.*

Keywords: *Adder, Low power, ETA, approximate part and accurate part.*

1. INTRODUCTION:

ETA consists of two parts, one is approximate part and another is accurate part. From the extensive analysis, it is observed that ETA can be further improved. The design can be further improved by modifying the architecture of approximate part over the existing architecture without any effect on the accuracy. In approximate part, addition is performed by Modified XOR gate as addition demands output to be '1' when both inputs are '1'. The Modified XOR gate requires at least 19 transistors. We have noticed that the same functionality can be achieved by our proposed adder with a very small amount of transistors (8 transistors only).

In the proposed work, the costly area inefficient Modified XOR is replace by the OR gate as it provides the same functionality with very small number of transistors. Including area efficient OR gate in place of Modified XOR significantly reduces area of the approximate part of the ETA. Thus overall there is significant reduction in power and delay metrics as well of the proposed approximate adder. In order to increase the speed performance of the adder via approximate adder.

2. PROPOSED APPROXIMATE ARCHITECTURE:

To improve all the design parameters simultaneously, we propose an efficient proposed approximate architecture in the least significant bits (LSB) positions. The approximate proposed adder is used to improve the design metrics. The architecture of proposed approximate adder is shown in Figure 1.1 that shows accurate and inaccurate parts as of ETA while both designs have same architecture but the only difference is that proposed OR gate is used in place of modified XOR gate. In the next section proposed approximate sum logic is discussed.

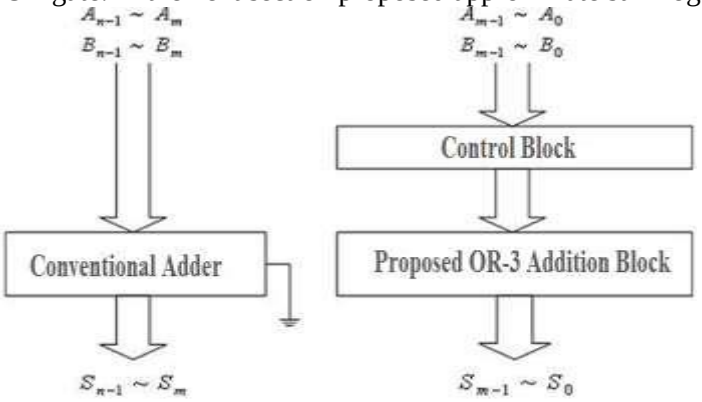

Figure 1.1: Architecture of proposed approximate adder

3. PROPOSED APPROXIMATE SUM LOGIC:

The symbol diagram of proposed approximate sum logic is shown in Figure 1.2. All the additions are performed by it and give the same result as of modified XOR in the ETA. This shows from the Figure that there are three inputs and one output. And the control signal is used as an input coming from the control blocks. Also architecture of multi-bit approximate addition logic is shown in further section.

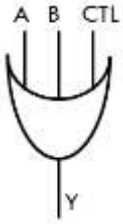

Figure 1.2 : Symbol of proposed approximate sum logic

4. ARCHITECTURE OF MULTI-BIT APPROXIMATE ADDITION LOGIC:

The architecture of multi-bit approximate addition logic is shown in the Figure 1.3 that shows OR gate is used in place of modified XOR gate and reduces area efficiently. All the addition is performed by multi-bit approximate addition logic. Since the functionality is same due to this it gives same results as got through modified XOR logic in the ETA.

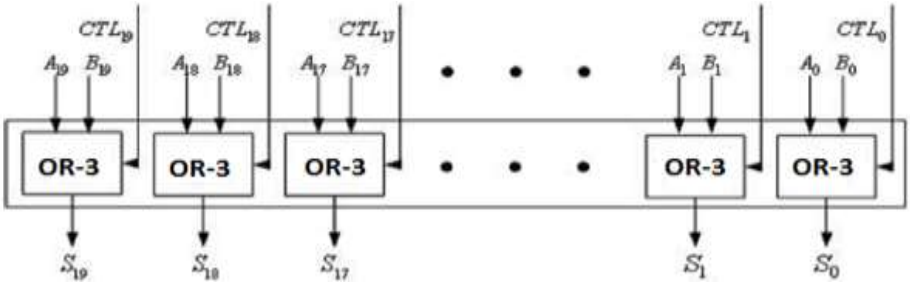

Figure 1.3: Architecture of multi-bit approximate addition logic

Thus, in our proposed work the implementation of approximate part via OR gate in place of modified XOR gate significantly reduces silicon area and this in turn reduces power consumption. By applying this, we achieve tremendous improvement in Area, power and delay simultaneously, which is the required energy efficient adder for error tolerant applications in the real time applications. The architecture proposed above provides significantly improved design metrics and error metrics that are acceptable by the different error tolerant applications.

5. IMPLEMENTATION OF PROPOSED APPROXIMATE ADDER:

The proposed and existing designs are implemented on Tanner to evaluate the design metrics. The schematic of the full adder which is used to construct RCA is shown in Figure 1.4. The full adder requires 28 transistors to generate sum bit and carry bit. Further, the full adder schematic utilizes the static CMOS logic to implement the functionality of the full adder. The sizes of the transistors are taken appropriately. Since the same full adder is used to construct other accurate and approximate adders of different bit-width, the designs can be compared effectively as each design will provides metrics due to its design style not because of transistor sizing. This full adder is also utilized to design the accurate adder part of the both ETA-I and the proposed adders.

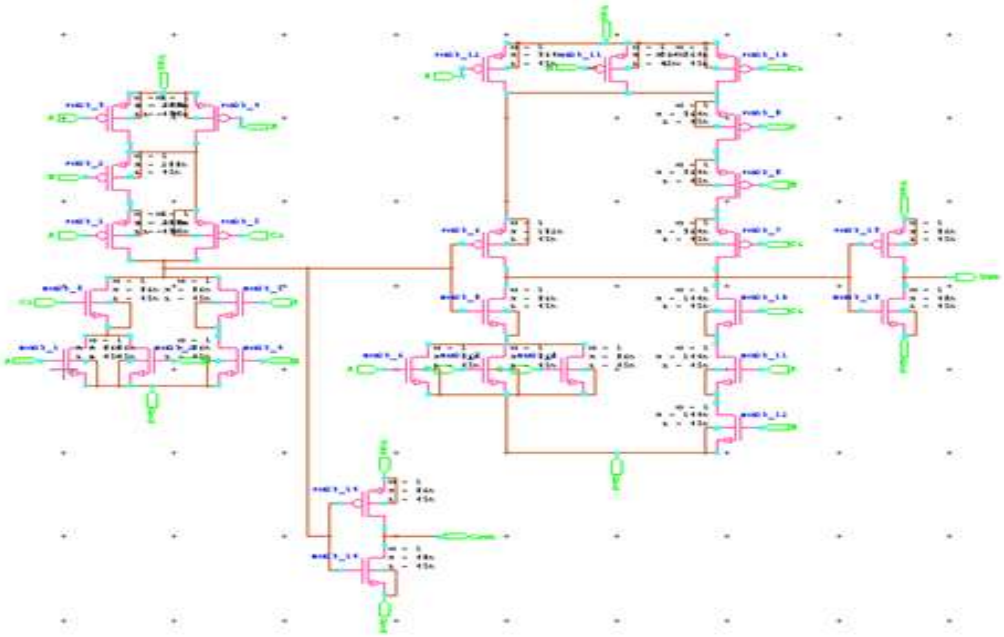

Figure 1.4: Schematic diagram of 28 transistors full adder.

The proposed approximate architecture is implemented on Tanner to evaluate the design metrics. For example, the schematic of the proposed approximate adder is further shown for all the adders respectively. The schematic diagram of 8-bit proposed approximate adder as shown in the Figure 1.5 illustrates that it exhibits 4-bit accurate and inaccurate parts.

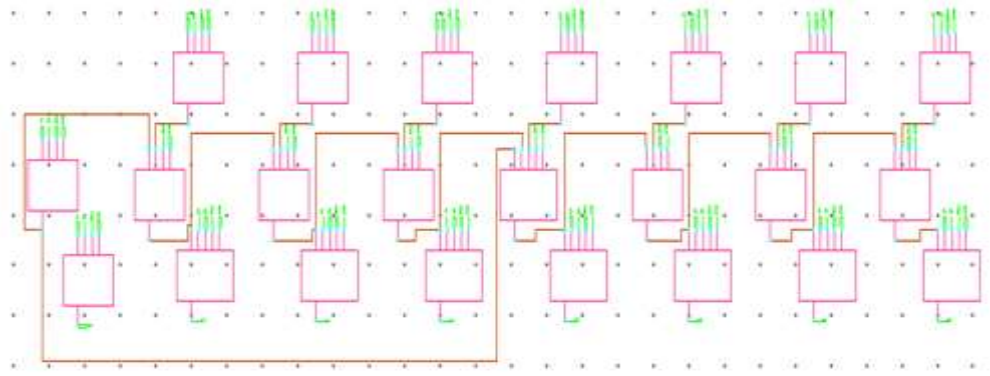

Figure 1.4: Schematic diagram of 8-bit proposed adder

The schematic diagram of 16-bit proposed approximate adder as shown in the Figure 1.5 illustrates that it exhibits 8-bit accurate and inaccurate parts. Similarly, the schematic diagram of 32-bit proposed approximate adder is shown in the Figure 1.5 that exhibits 16-bit accurate and inaccurate parts.

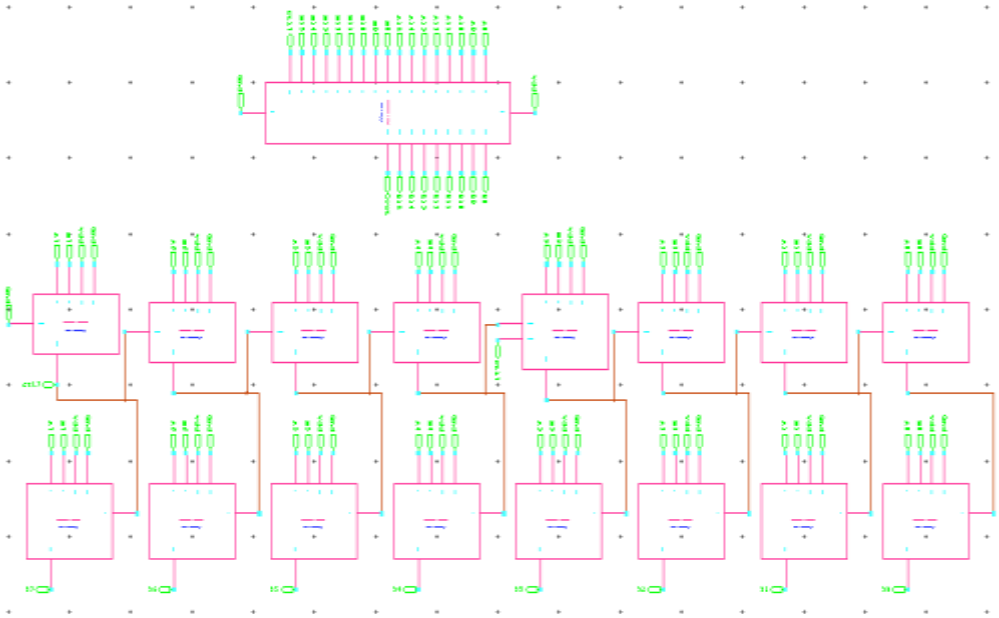

Figure 1.5: Schematic diagram of 16-bit proposed adder

Similarly, the schematic of the 32-bit proposed approximate adder is shown in the Figure 1.6 that exhibits 16-bit accurate and inaccurate parts.

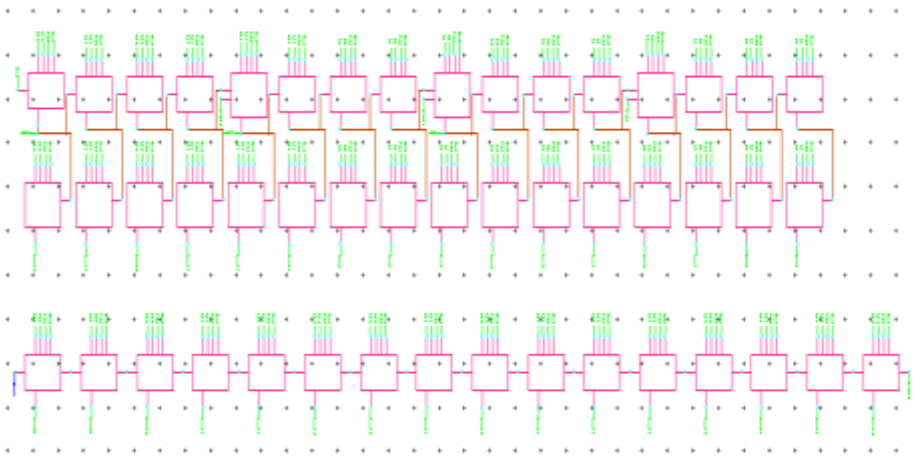

Figure 1.6: Schematic diagram of 32-bit proposed adder

6. RESULTS:

Table 1.1: Design metrics of 32-bit adders

Adders	Power (mW)	Delay (ns)	PDP (fJ)	# Transistor
RCA	0.027	1.33	0.03591	896
ETA-I	6.41	0.656	4.20496	854
Prop	2.89	0.656	1.89584	710

Similarly, comparing all the design metric of different adders through Table 1.1 we conclude that our proposed 32-bit adder requires **20.7%,** and **16.8%** reduces area over RCA, and ETA-I respectively. It can also be observed that proposed adder reduces delay by 50**%** over RCA. Thus, we can say proposed adder provides significant improvement in area and delay over all existing adders.

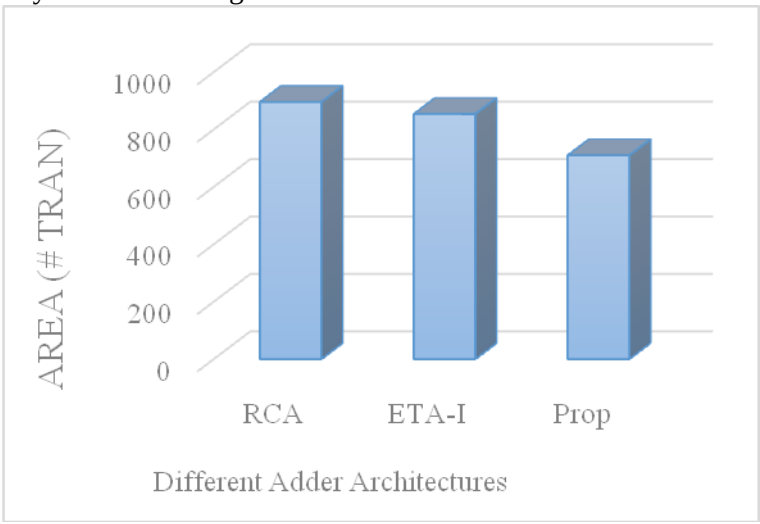

Figure 1.7: Area comparison of 16-bit design

Similarly, Figure 1.8 compares the delay of different adder architecture where proposed adder shows delay over the existing RCA adder. Thus, it can be used for those circuits that require high performance.

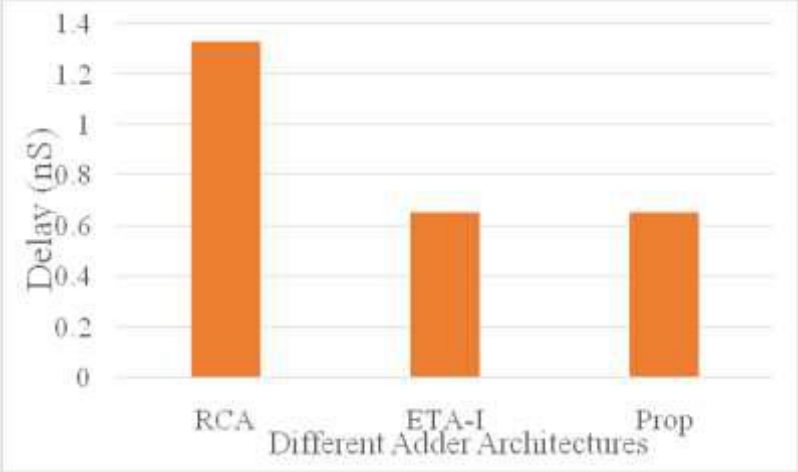

Figure 1.8: Comparison of 16-bit design metrics with Power

Thus from the simulation results, it can be observed that proposed design provides efficient design metrics without severe degradation in the output quality that matches to ITRS prediction [1]. All these achievements by proposed approximate adders makes it suitable for many error tolerant applications and effectively utilized in the portable battery operated devices where power/energy is the prime requirement over accuracy. Next section introduces about error metrics of proposed designs.

7. ERROR METRICS FOR THE APPROXIMATE DESIGNS:

The error metrics are evaluated by modelling the proposed adder on the MATLAB and simulating the design for 1 lakh random input pattern. The following error metrics are used to evaluate the approximate designs [2], [31], [32]:

Mean Error

Mean is nothing but the average of all the numbers. The mathematical expression for mean is given by Equation 1.1.

$$Mean\ (\mu) = {(E_1 + E_1 + E_1 + \cdots E_n)}/{n} \qquad 1.1$$

Mean Square Error (MSE)

The Mean Square Error (MSE) is the most commonly used error metric used in the image processing applications. The mathematical expression for MSE represents the cumulative squared error between the compressed and the original image.

$$MSE = \frac{1}{m.n}\sum_{i=0}^{m-1}\sum_{j=0}^{n-1}[I(i,j) - K(i,j)]^2 \qquad 1.2$$

Peak Signal to Noise Ratio (PSNR)

It is the most commonly used metric in the image compression to quantify the amount of error in the image compared to the original. The higher value of the PSNR is always desirable. The mathematical expression for the PSNR depends on the value of the MSE and signal amplitude and is expressed by the equation 5.3. and is measured in decibel.

The PSNR (in dB) is defined as:

$$PSNR = 10.\log_{10}\frac{MAX_I^2}{MSE} \qquad 1.3$$

$$= 20.\log_{10}\frac{MAX_I}{\sqrt{MSE}}$$

$$= 20.\log_{10} MAX_I - 10.\log_{10} MSE$$

Here, MAX_I is the maximum possible pixel value of the image. When the pixels are represented using 8 bits per sample, this is 255.

8. QUALITY METRICS ANALYSIS:

The error metrics is shown in Table 1.2, which describes that 8-bit proposed adder, has less value of mean, whereas the value of 16 bit proposed adders is increasing. The quality metrics of the proposed adder is similar to the ETA-I adder as in the proposed adder no change in the control and sum generation logic while there is only change in the architectural design of the logic.

Table 1.2: Comparison of error metrics

Metrics	ETA-I		ETA-II		Proposed	
	8-bit	16-bit	8-bit	16-bit	8-bit	16-bit
Mean	0.0149	0.933	0.0368	0.0394	0.0149	0.933
MSE	$7.46\text{x}10^{-4}$	$4.07\text{x}10^{-5}$	0.0119	0.0122	$7.46\text{x}10^{-4}$	$4.07\text{x}10^{-5}$
Std. Dev.	0.0273	0.0064	0.1092	0.1103	0.0273	0.0064

However, all the proposed adders have less value of these quality metrics which is acceptable for most of the error tolerant applications. Thus, proposed adder is suitable for image processing.

9. CONCLUSION:

The simulation result shows that proposed adder outperform over the existing adder and can be effectively applied to the applications that can tolerate small amount of error. Consequently, it is obvious that our proposed adder for the approximate part can provides improved area, power, delay, and PDP simultaneously with minor loss in accuracy. From the simulation results it is also cleared that the design metrics shows significant reduction in area, power and delay over the accurate and approximate adder architectures. It is very convenient for multimedia applications which already contained small amount of errors. Thus, we can say that the proposed adder can be effectively utilized in the error tolerant applications such as in many DSP applications for portable devices.

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