INTERNATIONAL JOURNAL FOR INNOVATIVE RESEARCH IN MULTIDISCIPLINARY FIELD ISSN: 2455-0620 Volume - 5, Issue - 6, June – 2019
Monthly, Peer-Reviewed, Refereed, Indexed Journal with IC Value: 86.87 Scientific Journal Impact Factor: 6.497
Received on : 20/06/2019 Accepted on : 29/06/2019 Publication Date: 30/06/2019

Low Power SRAM Cell Design Using Gate Diffusion Input (GDI) Techniques

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Abstract: *Static Power dissipation due to memories has become a major issue of digital design. Scaling of CMOS technology has led to short channel effects. In this paper, VDD pre-charge and charge recycling technique for low power read operation was proposed. A 4T read port is designed and included in 10T proposed technique. Read BL (RBL) is charged and discharged through the read port according to the state of stored bit. Read port is powered by virtual power rails that run horizontal and are shared by the cells of a word. The dynamic control of read port power rails reduces the RBL leakage substantially The proposed 10T cell in a commercial 65 nm technology is 2.47× the size of 6T with β = 2, provides 2.3× read static noise margin, and reduces the read power dissipation by 50% than that of 6T. The value of RBL leakage is reduced by more than 3 orders of magnitude and (ION/IOFF) is greatly improved compared with the 6T BL leakage. The overall leakage characteristics of 6T and 10T are similar, and competitive performance is achieved. The SRAM cells designed with 30nm LG are used in multi-segment hybrid SRAM architecture. The results are compared with the original hybrid SRAM. It is observed that the energy metric of proposed architecture is 7% less compared to hybrid SRAM.*

Key Words: *Delay, GDI, Power, ,Spice., SRAM, Tanner*

1. INTRODUCTION:

Static RAM memories (SRAMs) are hardware search engines that are much faster than algorithmic approaches for search-intensive applications. SRAMs are composed of conventional semiconductor memory (usually SRAM) with added comparison circuitry that enables a search operation to complete in a single clock cycle. The two most common search-intensive tasks that use SRAMs are packet forwarding and packet classification in Internet routers. I introduce SRAM architecture and circuits by first describing the application of address lookup in Internet routers. Then we describe how to implement this lookup function with SRAM.[1]

2. SRAM CIRCUITS:

2.1 6T SRAM Circuits

Figure 1 displays a conventional SRAM core cell that stores data using positive feedback in back-to-back inverters. Two access transistors connect the bit lines, bl and /bl (we use the prefix / to denote the logical complement in the text and we use an overbear in the figures), to the storage nodes under control of the word line, wl. Data can be read from the cell or written into the cell through the bit lines. Use this differential cell as the storage for building SRAM cells. Figure 2 depicts a conventional binary SRAM (BSRAM) cell with the match line denoted ml and the differential search lines denoted sland /sl. The figure also lists the truth value, T, stored in the cell based on the values of d and d. Read and write access circuitry is omitted for clarity in this figure and subsequent SRAM core cell figures[2].

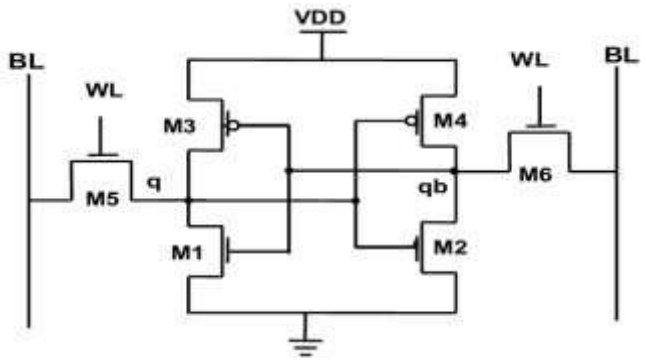

Figure 1. conventional 6T SRAM core cell

2.2 Binary SRAM (BSRAM)

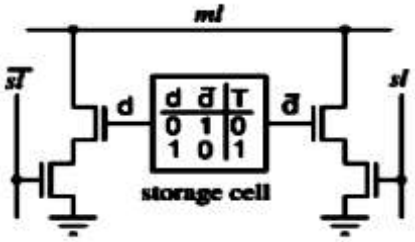

Figure 2. Conventional BSRAM core cell

For a binary SRAM, we store a single bit differentially. The comparison circuitry attached to the storage cell performs a comparison between the data on the search lines (sl and /sl) and the data in the binary cell with an XNOR operation (ml = ! (d XOR sl)). A mismatch in a cell creates a path to ground from the match line through one of the series transistor pairs. A match of d and sl disconnects the match line from ground.

Conventional SRAM storage cell, binary SRAM and ternary SRAM cells. The SRAM cells omit the read/write access circuitry for clarity[13].

2.3 Match line of a NOR-based SRAM

A mismatch of any of the bits on the match line discharges the match line; an example discharge path is shown in the figure.4. A match results in the match line remaining in the precharge state which occurs if all bits in a word match.[3]

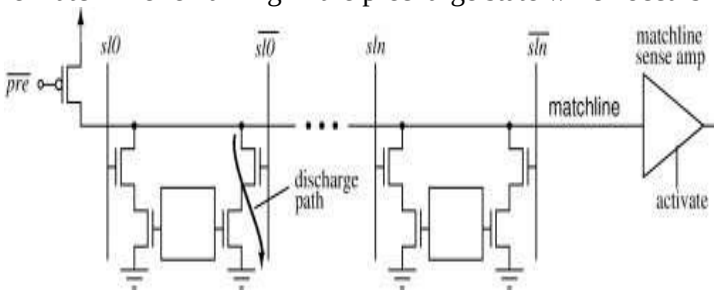

Figure.3. The match line of a NOR-based SRAM

In typical use, a SRAM has only one or a small number of matches and most words mismatch. Since mismatches dominate, most match lines transition both during precharge and during evaluation. This leads to a high power consumption on the match lines. Further, the search-lines, which broadcast the data to the SRAM cells are highly capacitive[9]. The search-lines are another large source of power dissipation in SRAM. Because of these large sources of power dissipation, recent research in SRAM design focuses on circuit techniques for reducing power consumption.

3. METHOD:

3.1 Gate Diffusion Input

The three inputs in GDI are namely1) G- common inputs to the gate of NMOS and PMOS 2) N- input to the source/drain of NMOS 3) P- input to the source/drain of PMOS Bulks of both NMOS and PMOS are connected to N or P (respectively), that is it can be arbitrarily biased unlike in CMOS inverter. The important difference between CMOS and GDI is that in GDI N, P and G terminals will given a supply 'VDD' or can be grounded or can be supplied with input signal based upon the circuit to be designed and hence effectively minimizing the number of transistors used in case of most logic circuits (eg. AND, OR, XOR, MUX, etc).

3.2 L-EDIT PRO (BACK END EDIT)

Tanner EDA's L-Edit Pro is a comprehensive physical layout and verification system that accelerates design cycles by combining the fastest rendering available with powerful features that exceed the needs of the most demanding user[6]. We have added a 4T read port to the 6T cell to decouple the internal nodes during the read operation. Read port consists of an INV P1-N1 driven by node QB, and a transmission gate (TG) P2-N2. The output (Z) of the INV is connected to RBL during the read operation through TG, which is controlled by (read) control signals.

4. PROPOSED SRAM CELL

4.1 8T SRAM

A novel 8T SRAM cell structure to the leakage current and dynamic power consumption has been reported in this work. The schematic of proposed 8T SRAM cell at 65nm technology is as shown in figure. 7. The proposed SRAM cell composed of write access transistor (M3), controlled by Write Word Line (WWL) and read access transistor (M8) is controlled by the Read Word Line (RWL). During the write operation WWL is transitions to high value and RWL and BLB both are maintained at Hence, the read access transistor (M8) cut OFF. To write „1" into the cell Bit Line (BL) is pre charged to a high value, then „1" is forced through the write access transistor (M3). Similarly, to write „0" into the cell, BL is discharged.

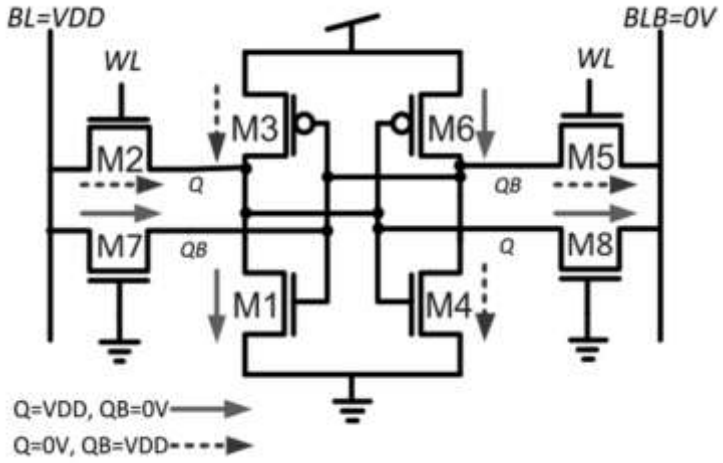

Figure.5. 8T SRAM cell at 65nm technology

Hence, to perform write operation the proposed cell utilizing single BL, which could leads to reduction in the dynamic power consumption and leakage power. with technology scaling below nanometer the power dissipation of 6T SRAM becomes significant with low power supplies as due to this the gate delay is increased which reduces the frequency of operations. An 8T SRAM cell with charge sharing technique which used at architecture level is implemented at the cell level of design. Due to this Stack Transistors the power dissipation has reduced from 18 % in comparison to Conventional 6T SRAM cell. The 8T SRAM provides power efficient solution. in 8T SRAM cell is 30 % faster then conventional SRAM cell ,this can be acheived by cahnge in delay constrainsts and low power SRAM cell consume lesser power

4.2 10T SRAM

The 10T SRAM cell using an INV and a TG has been proposed earlier [5]. However, the proposed 10T scheme is different from the previous design in the following aspects. 1) The previous INV+TG-based 10T cell was application specific, while our proposed design is generic[7]. 2) We have used the dynamically controlled power rails for the read port. 3) We precharge RBL at VDD/2, while the previous 10T design eliminated the precharge phase, and used INV to fully charge or discharge the RBL. 4) The basic read technique of both the designs is completely different[4].

LP10T) is precharged by VP supply, which has a value half that of the supply voltage.

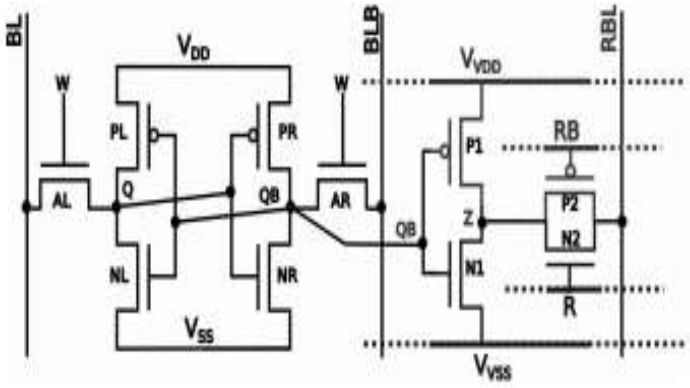

Figure.6. 8T SRAM cell at 65nm technology

The main idea of the proposed design[11] is "the charging or the discharging of the read BL from VDD/2 for every read operation." The previous design either discharges from VDD to VSS, or charges from VSS to VDD. 5) A powerful INV was used previously to produce full VDD swing on the RBL. In this proposed SRAM , RBL is precharged at VDD/2, and only a small voltage difference in 6T is produced for every read cycle) In the proposed design, for every read cycle the RBL will exhibit some change (positive or negative) from its precharged value of vdd/2[8]. However, in , the RBLPrecharging and Read Operation The proposed 10T SRAM (hereafter referred to as LP10T) is precharged by VP supply, which has a value half that of the supply voltage..

5. ANALYSIS:

Power Consumption for the modified SRAM cell are shown in the below table

Table.1 POWER CONSUMPTION TABLE

Design	Power (mW)	Delay (sec)
6T	7.43	1.22
8T	8.6	0.81
10T	4.1	1.28

6. SIMULATION RESULT:

The figure shows the simulation waveform for 6T SRAM cell

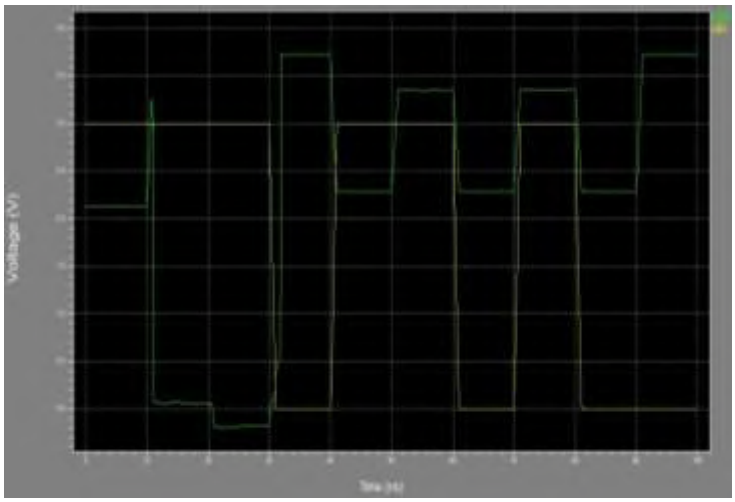

Figure 7. 6T SRAM Waveform

The figure shows the simulation waveform for 8T SRAM cell

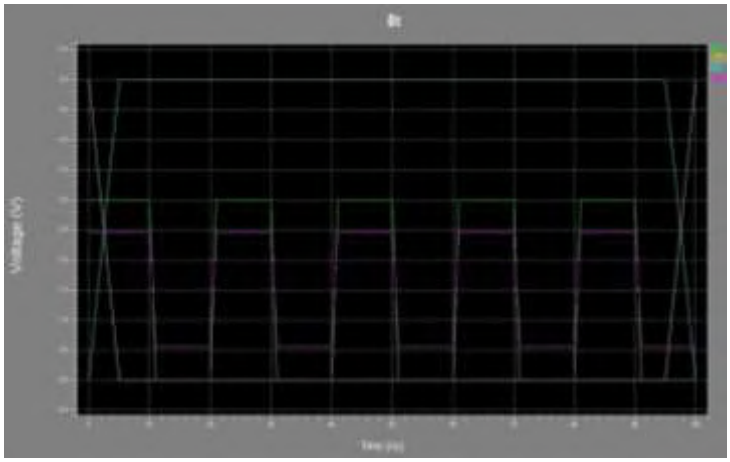

Figure 8. 8T SRAM Waveform

The figure shows the simulation waveform for 10T SRAM cell

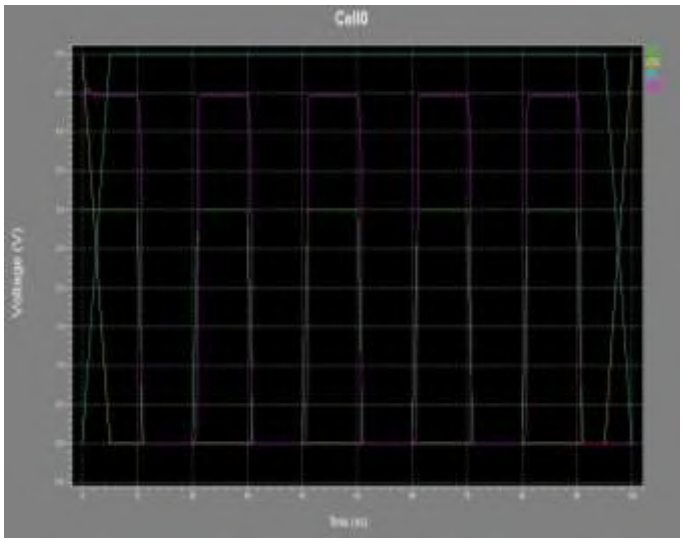

Figure 9. 10T SRAM WAVEFORM

7. CONCLUSION:

The 8T & 10T SRAM cell is designed in CMOS technology and its performance characteristic has been analyzed. The designed 8T & 10T SRAM has write capability as good as 6T SRAM and improved read stability than 6T SRAM cell. The power dissipation, delay, and power delay product of the designed 8T & 10T SRAM cell has been shown in the above figures. The power consumption of 6T, 8T and 10T for read and operation has been calculated. The power consumption of 10T SRAM cell and 10T using GDI (Gate Diffusion Input) techniques becomes less when compared to 6T SRAM cell. But 8T SRAM cell exhibited increased leakage power consumptions for both data levels.

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