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Rising FinFET Technology over current CMOS Technology in Analog Circuits

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Abstract: *Differential amplifiers are a crucial facet in many analogue systems. Centered on 16 nm FinFET technologies, this paper proposes a concept for a Single Stage Differential Amplifier. We engineered a differential amplifier with Slew Rate, Gain, CMRR, Unity Gain Bandwidth, and Frequency Response, and compared it to 16 nm differential amplifiers using traditional MOSFET, FinFET, and CNFET. With a supply voltage of 1.0V, the proposed standard Single Stage Differential Amplifier produces an open loop gain of 18.19 dB, a Slew Rate of 7.74E+6 V/sec, and a Unity Gain Bandwidth of 249 MHz. Hspice simulation software is used for all simulations. The simulations show that the Fin FET circuit outperforms the MOSFET and CNFET circuits in terms of Gain, CMRR, and Slew Rate at this period.*

Key Words: *Differential amplifier; MOSFET; Cutoff frequency; Slew Rate; CNFET; Independently Driven Double Gate (IDDG);* C_L *(Load Capacitance).*

1. INTRODUCTION:

Computer measurements are being moved to the Decca-nanometer by CMOS scaling. This will necessitate the use of novel materials and device architectures in order to reap the benefits of device scaling in terms of device efficiency [1].

To render available extensions, a variety of technical and system structure variants will be proposed, such as single gate FETs, SOI FETs, multiple-gate FETs, and CNFETs, among others. FinFETs and CNFETs, for example, have recently become important technologies for low-power, low-voltage applications. Because of their higher electrostatics, flexibility, and stability, Double Gate based transistors will eventually replace CMOS. Differential amplifiers play a crucial role in analogue circuits [2]. Carbon nanotubes are unique in that they are one of the few schemes in which the investigational system measurements can be reduced to very small versions. Might match the predictions, allowing, in theory, for the experimental justification of computational methods and device schemes [3].

It is critical to design exceptional enactment analogue integrated circuits with low supply voltages. There is a trade- off between Power, Slew Rate, Gain, and other performance parameters at extremely high supply voltages. We will focus on the design and analysis of low-power, low-voltage Single Stage Differential Amplifiers using MOSFET, CNFET, and FinFET technology in this paper. FinFET-based differential amplifier simulation results are compared to those of traditional CMOS and CNFET-based differential amplifiers. The simulations are run on all three device types, MOSFET, CNFET, and FinFET, and the results are compared for the best result for each device type.

2. DG-FINFET AND CNFET DEVICE STRUCTURE:

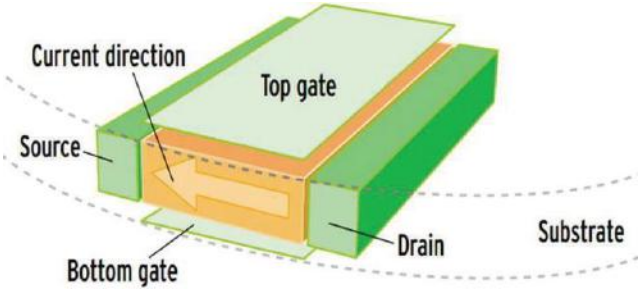

Figure 1(a):. FinFET Structure [4].

At Nanometer technology, a FinFET transistor has the ability to exchange bulk devices [4, 5]. FinFET is a dual gated MOS scheme that leads to higher enactment because it is less susceptible to the short channel effect [11]. FinFETs are expected to replace MOSFETs because they are better at controlling drip and reducing short channel

effects while still maintaining a strong current [12].

Figure 1(a) illustrates the FinFET structure. FinFETs are configured as 3T (three-terminal) devices with either gates shorted, or 4T (four-terminal) devices with one gate fixed, gate bias, and the control terminal the facade gate [11, 12]. Prior studies have evaluated FinFET advancements, concluding that FinFETs are appealing for RF, low power, and low frequency applications [1, 5]. The three-terminal symmetric FinFET is well-designed in comparison to other structures for enhanced drive current capability[4,12].

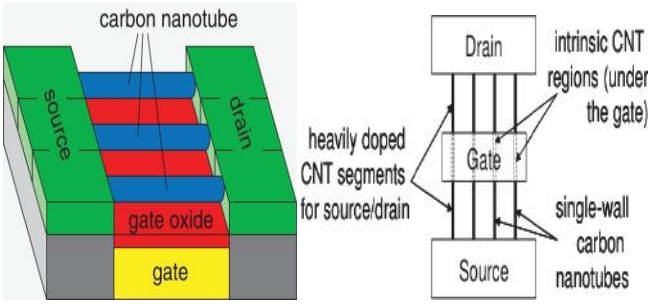

Figure 1(b):. CNFET Structure [6,12].

CNT is made by rolling a pane of graphite along a wrap vector. Depending on the chirality vector, metallic or semiconducting materials are used. SWCNTs (single-walled carbon nanotubes) may be available [6]. Single or several semiconducting SWCNTs are castoff in a Carbon Nanotube Field Effect Transistor. The device's channel is depicted in Figure 1 (b). The diameter of a carbon Nanotube is expressed as a chirality vector. The chirality vector is expressed in terms of an index (n, m), where m, n is the pair of integers that expresses it. The diameter of a nanotube (Dt) in terms of n and m is given below. In the intermolecular distance between each carbon atom and another adjacent atom, ao = 0.142nm [9,12].

$$Dt = \frac{\sqrt{3a0}}{v}\sqrt{m^2 + mn + n^2} \quad (1)$$

In consideration of the precise format example and capacitance of interconnect wiring, the circuits using CMOS and the circuits using CNFET with per system 1 to 10 carbon nanotubes are about two to ten times faster, the per cycle expending vitality is about seven to two times less, and the Power delay product exists adjacent twenty to fifteen times second rate [7].

3. SCHEME OF SINGLE STAGE DIFFERENTIAL AMPLIFIER CIRCUIT:

In this area, we understood three adaptations of the differential amplifiers supported the CMOS, CNFET and FinFET technology at 16 nm node. Synopsys HSPICE was used as a circuit simulator. Figure 2 shows a FinFET-based Single Stage Differential Amplifier.

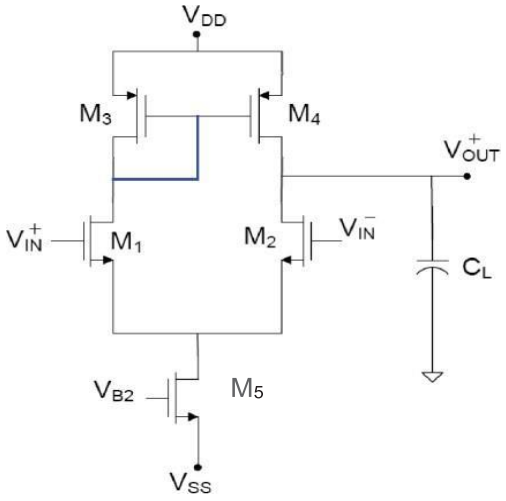

Figure 2: Single-Stage Differential Amplifier.

The ideal basic system parameters for a CNFET-based differential amplifier circuit are the number of nanotubes (N), inter nanotube spacing pitch (S), CNT diameter, and input supply voltage (V) [2, 11]. The sizing of the transistors to meet the desired output and electrical characteristics is the primary outline concern for the analogue

designer when handling a CNFET technology. The W and L of the transistors are the optimization variables in CMOS and FinFET , while N, S and V are the variables in CNFET. Table 1 lists the values for the differential amplifier scheme variables for FinFET, CMOS and CNFET.

Table 1. Optimized Circuit Parameters and it's Value of CMOS, CNFET And FinFET.

Parameter	CMOS 16nm		CNFET 16nm		FinFET 16nm	
	L	W	S	N	L	W
M_1	16nm	12µm	18	3	16nm	50µm
M_2	16nm	12µm	18	3	16nm	50µm
M_3	16nm	60µm	18	3	16nm	50µm
M_4	16nm	60µm	18	3	16nm	10µm
M_5	16nm	150µm	18	3	16nm	150µm
C_L	1 FF		1 FF		1 FF	

4. SIMULATION RESULTS ANALYSIS AND COMPARSION:

All of the parameters mentioned above are used to determine the output of a differential amplifier. The three differential amplifiers' performance characteristics and robustness are thoroughly investigated in terms of circuit specifications, such as SR (Slew Rate), open loop Gain, CMRR (common-mode rejection ratio), Frequency Response, and Unity Gain Bandwidth. Simulating the circuits at 1.0 V and 1.8 V VDD supplies yields the differential amplifier's output characteristics. Below are all of the stimulated diagrams.

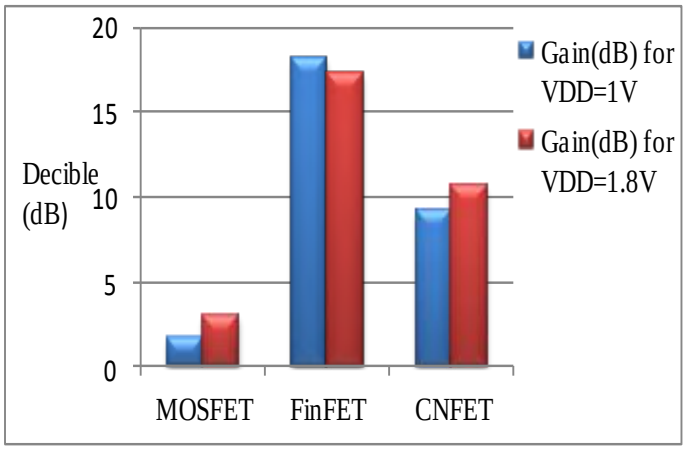

Figure 3: Gain of Differential Amplifier in dB.

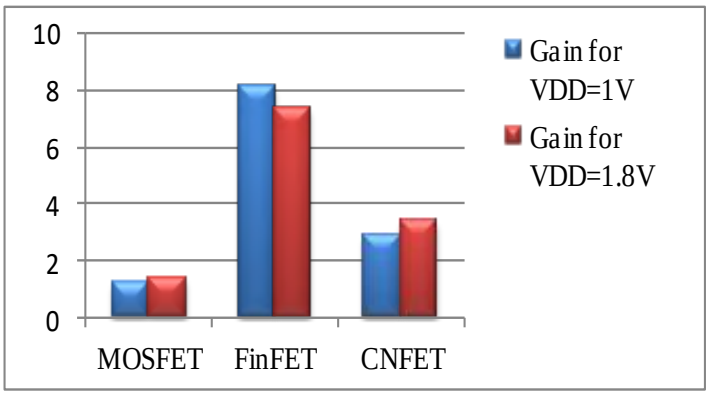

Figure 4:. Gain of Differential Amplifier.

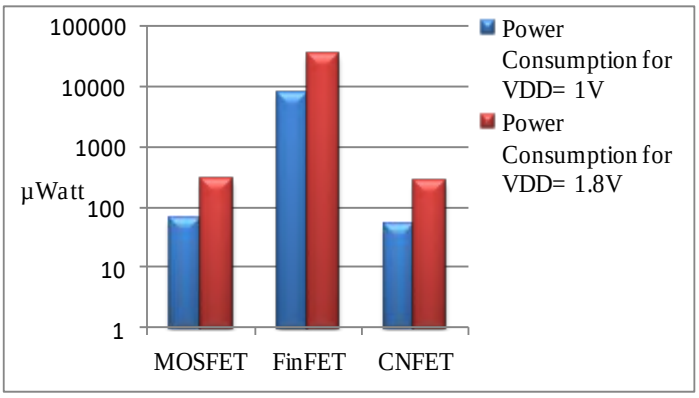

***Figure 5**:* Power Consumption of Differential Amplifier.

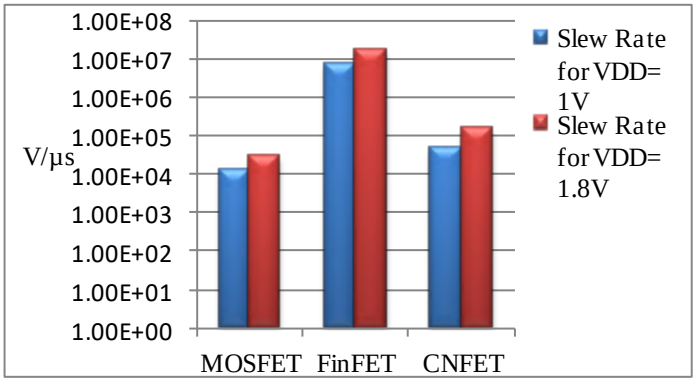

***Figure 6**:* Slew Rate of Differential Amplifier.

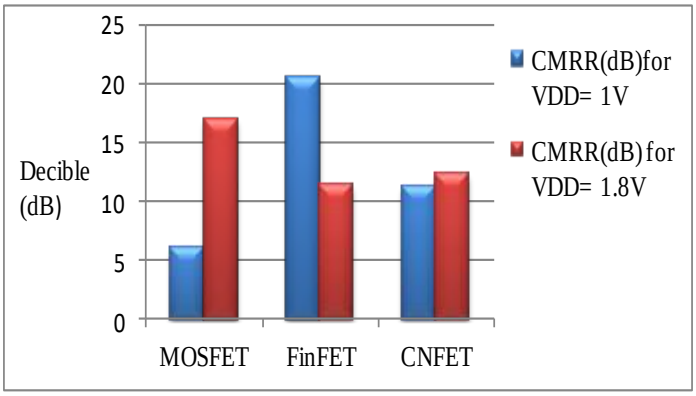

Figure 7: CMRR of Differential Amplifier.

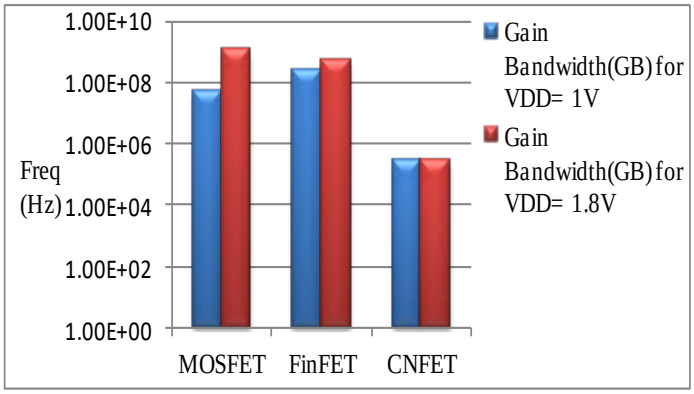

***Figure 8**:* GB product of Differential Amplifier.

Table 2 shows the modeled effects of the proposed FinFET, CNFET, and MOSFET centered differential

amplifiers, while Figure 3, 4, 5, 6, 7 and 8 display comparative graphs of Gain (dB), Gain, Power Consumption, Slew Rate, CMRR, and Unity Gain Bandwidth . The simulation results show that FinFET differential amplifiers have a significant improvement in terms of gain, slew rate, and CMRR, but that their power consumption is higher than traditional 16-nm CMOS and CNFET differential amplifiers. Differential amplifiers using FinFET, gain and slew rate increase at lower supply voltages than at 1.8 VDD. Furthermore, differential amplifier power consumption is reduced at lower supply voltage. Low Power Consumption Differential Amplifier Using 16 nm CNFET. The biasing current is responsible for the majority of the power consumption in a differential amplifier. In this way, the power consumption of a FinFET system can be reduced even further by lowering the biasing current and adjusting the W/L proportion appropriately. Carbon Nanotubes one-dimensional nature prevents carrier scattering and dangling bonds, lowering the power consumption of CNFET devices.

Table 2. Comparison of CNFET, MOSFET AND FinFET Differential Amplifier.

Parameters	16 nm CNFET		16 nm MOSFET		16 nm FinFET		[8]	[10]
V_{DD} (V)	1.0	1.8	1.0	1.8	1.0	1.8	1.0	1.0
Gain	2.9	3.41	1.21	1.41	8.12	7.33	25.11	….
Gain (dB)	9.24	10.65	1.65	2.98	18.19	17.30	28	59
Frequency Response(Hz)	104K	97.7K	22.7M	402M	51.2M	216M	10 G	….
Slew Rate (V/µsec)	49900	153040	13000	30450	7.74E+6	182e+5	….	….
CMRR(dB)	11.31	12.26	6.1050	16.99	20.55	11.34	70-90	….
Unity Gain Bandwidth(Hz)	261K	278K	48.3M	1200 M	249M	541 M	….	3.5G
Power Consumption (µWatt)	50.1	275	64.3	279.2	7460	34200	77	10

5. CONCLUSION:

The advantages of rising FinFET technology over current CMOS technology in analogue circuits are explored in this paper. CNFETs have come a long way in the interim of the main breakthrough, establishing their dominance over traditional devices. We conclude that the CNFET version has lower power consumption, better gain, and slew rate than the MOSFET version, and the frequency response of the CNFET-based differential amplifier is lower than the MOSFET version. The key impact of this paper is the strong link between emerging innovations; in particular, CNFET and FinFET are contenders to challenge CMOS devices designed for low-power analogue circuits. A method for reducing the power consumption in FinFET and improving the frequency reaction of CNFET for differential amplifiers can be investigated further.

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